

REMARKS

Claims 1-5, 7-9, 11, 13-23, and 29-34 remain in the application for consideration of the Examiner with Claims 24-28 standing withdrawn.

Reconsideration and withdrawal of the outstanding objections and rejections are respectfully requested in light of the following remarks.

Applicants appreciate the indication that the proposed drawing correction has been approved.

Formal drawing corrections have been included by separate letter.

Claim 2 was rejected under 35 U.S.C. § 112, second paragraph.

This rejection is traversed.

The Examiner alleges that the symbol "□" is not based on any standard.

However, the basis under 35 U.S.C. § 112 is not whether or not it is based on a standard but if the claim language has particularly pointed out and distinctly claimed the subject matter which Applicant regards as their invention. Here, Applicants have done that.

It is respectfully submitted that Claims 1-5, 7-9, 11, 13-23, and 29-34 particularly point out and distinctly claim the subject matter which Applicants believe is their invention.

Turning now to the art rejection, Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Yamasaki; Claims 2 and 3 were rejected under 35 U.S.C. § 103 as being unpatentable over Yamasaki; Claims 4, 5, 7, 8, 11, 15, 20, 21, and 23 were

rejected under 35 U.S.C. § 103 as being unpatentable over Yamasaki in view of Tani; Claim 9 was rejected under 35 U.S.C. § 103 as being unpatentable over Yamasaki in view of Tani in view of alleged Applicants admitted prior art; and Claims 13, 20, and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over Yamasaki in view of Tani in view of Wolf.

These rejections are respectfully traversed.

It is respectfully submitted that Yamasaki does not disclose or suggest the presently claimed invention including the network of power distribution lines deposit on the surface of the chip, over active components of the circuit, albeit defined as electrically conductive films pattern into a network of lines substantially vertically over the active components in independent Claim 4.

The Examiner alleges that Yamasaki discloses in element 70 an active component.

However, the Examiner's attention is directed to column 2, lines 53-55 where Yamasaki discloses that element 70 is a noise removing capacitor.

Tani does not disclose or suggest the presently claimed invention including the network or power distribution lines deposit on the surface of the chip over active components of the circuit as defined in the various forms in independent Claims 1 and 4.

There is nothing in Tani to suggest this feature.

Whether or not the alleged admitted prior art discloses that it is common practice to manufacture single piece lead frames from a thin sheet of metal or whether one of ordinary skill in the art would consider modifying either Yamasaki or Tani is of no

moment since the result in construction would still in no way disclose or suggest the presently claimed invention.

Wolf does not cure the above noted defects.

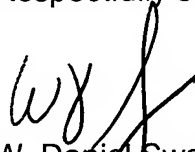
Applicants appreciate the indication that Claims 29-34 are allowed.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'W. Daniel Swayze, Jr.', written over the typed name.

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